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PATENT

Case Docket No. MICRON.170A
Date: December 15, 2003

In re application of	:	Paul A. Farrar
Appl. No.	:	09/909,181
Filed	:	July 19, 2001
For	:	METHOD OF USING FOAMED INSULATORS IN THREE DIMENSIONAL MULTICHIP STRUCTURES
Examiner	:	Chris C. Chu
Art Unit	:	2815

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

16 December 2003
(Date)

Linda H. Liu, Reg. No. 51,240

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is an Appellants' Brief to the Board of Patent Appeals:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Paul A. Farrar
Appl. No.	:	09/909,181
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Group Art Unit	:	2815

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES
APPELLANT'S BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant, in the above-captioned patent application, appeals the rejection of Claims 1-26 which were rejected in the Office Action mailed July 16, 2003. This appeal brief is filed in triplicate.

I. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

No appeals or interferences related to this case is currently pending.

III. STATUS OF CLAIMS

Claims 1-26 are pending and are appealed.

Claims 27-32 have been restricted out.

IV. STATUS OF AMENDMENTS

The claims presently on appeal are the claims Applicant filed in the Advisory Action response mailed on May 1, 2003.

V. SUMMARY OF THE INVENTION

The present invention concerns a high density multi-chip cube structure having reduced capacitive coupling between electrical interconnects, summarized at page 3, lines 10-29 and page 4, lines 1-24. The multi-chip cube structure includes a foamed insulating layer interposed between adjacent chips to provide electrical isolation between adjacent chips. Page 4, lines 5-8. The foamed insulating layer has a plurality of enclosed regions of air dispersed therethrough such that the dielectric constant of the insulating layer is reduced to less than that of the insulating material, which in turn reduces the capacitive coupling between conductors on adjacent chips. Page 4, lines 14-16. Consequently, the chip insulating layer has a lower dielectric constant and yet still retains most of the physical and mechanical advantages afforded by insulating layers made with conventional insulating material. Page 5, lines 11-13. In one embodiment, the insulating material is a foamed polymeric material. Page 4, lines 5-6. In another embodiment, the enclosed regions of air in the insulating material are each less than the width of the space separating adjacent conductors. Page 7, lines 10-12.

VI. ISSUES PRESENTED ON APPEAL

The following issues are presented:

Whether Claims 1-26 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Asada (U.S. Pat. No. 6,239,496) in view of Hiraoka et al. (U.S. Pat. No. 6,465,742).

Whether Claims 1 and 19 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Bertin et al. (U.S. Pat. No. 5,478,781) in view of Hiraoka et al. (U.S. Pat. No. 6,465,742).

Whether Claims 1-26 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Bertin et al. (U.S. Pat. No. 5,478,781) in view of Farrar (U.S. Pat. No. 6,077,792.

VII. GROUPING OF THE CLAIMS

In the present case, the rejected claims do not all stand or fall together. Applicant submits that each claim presents distinct issues concerning patentability. In the interest of administrative economy and efficiency, however, Applicant agrees to narrow the issues for the purpose of this appeal by grouping the claims as follows:

GROUP I: Claims 1, 3, 5-10, 12-18 which relate generally to a multi-chip cube structure having a foamed chip insulating layer disposed between adjacent chips, wherein the foamed chip insulating layer has a plurality of enclosed regions of air dispersed within and throughout the insulating material such that the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material, which in turn reduces the capacitive loading between chips in the multi-chip cube structure.

GROUP II: Claims 2, 4, 11, 19-26 which are directed generally to the same subject matter as Claims 1, 3, 5-10, 12-18 but which relate to a multi-chip cube structure having a foamed conductor insulating layer, wherein the foamed conductor insulating layer provides electrical isolation between adjacent conductors on the same chip, wherein the conductor insulating layer also has a plurality of enclosed regions of air dispersed within and throughout the insulating material such that the dielectric constant of the conductor insulating layer is less than the dielectric constant of the insulating material.

VIII. ARGUMENT

A. None Of The References Cited By The Examiner, Either Alone Or In Combination, Teach A Multi-chip Cube Structure Incorporating An Insulating Layer Having Enclosed Regions Of Air Dispersed Therethrough To Lower The Dielectric Constant Of The Insulating Layer.

Applicant claims a multi-chip high density semiconductor structure having an insulating layer disposed between chips, wherein the insulating layer has a plurality of enclosed regions of air dispersed therethrough. (See, *e.g.*, Claim 1) The enclosed regions of air are formed in the insulating material to lower the dielectric constant of the insulating layer, which advantageously reduces capacitive coupling between adjacent chips without substantially compromising the physical and mechanical advantages afforded by the insulating layer. In a preferred embodiment, the insulating layer comprises a foamed polymeric material, which has a lower dielectric constant

and yet retains substantially the same mechanical and physical properties as conventional polymeric materials. This is particularly advantageous in the context of multi-chip semiconductor modules, such as multi-chip cube structures, in which it is desirable to have a chip insulating layer with a low dielectric constant and yet sufficient load bearing capacity so as to provide mechanical support for additional chips in the module or to withstand the shear forces exerted on the module during assembly. None of references cited by the Examiner claim such an invention.

In the Office Action mailed July 16, 2003, the Examiner indicated that Applicant's invention is obvious in light of Asada in view of Hiraoka. However, Applicant notes that Asada is concerned with reducing the overall height of a multi-chip module (MCM) and stacking the chips in a manner so that the MCM can better withstand stress and resist cracking. Asada does not at all address the problem associated with capacitive coupling between chips in a chip stack. In fact, the MCM structure shown in Asada is unlikely to have any significant capacitive coupling problems between adjacent chips because the adjacent chips are separated by a sufficiently wide distance comprising the thickness of the insulating substrate 601 and a resin layer 621 (See, *e.g.*, Figure 8B of Asada)

Moreover, it would be counter-intuitive to form enclosed regions of air in the insulating substrate described in Asada. According to Asada, the insulating substrate is comprised of a "tape-like insulation polymer film" that is laminated to a copper thin film whereby patterning is carried out so as to delineate plural patterns of the copper wiring on the insulating substrate. (See, *e.g.*, Column 15, Lines 27-54 of Asada) The formation of voids in the insulating substrate is likely to cause the copper wiring to delaminate from the insulating substrate in regions where the voids are present in the interface between the substrate and the metal wiring, which can ultimately cause the module to malfunction. Accordingly, not only does the MCM structure recited in Asada appear not to have a significant capacitive coupling problem that is being addressed by Applicant's invention, the manner in which Applicant's invention is proposing to reduce capacitive coupling can actually be detrimental to the MCM described in Asada.

Moreover, there would have been no motivation to incorporate the porous material described in Hiraoka to the MCM disclosed in Asada. Hiraoka is directed toward a photonic crystal used in a light functional element such as a branching filter, an optical waveguide, a light

delay element, etc. (See, *e.g.*, column 1, lines 13-25 of Hiraoka) In fact, the only remote relevance Hiraoka appears to have in relation to Applicant's invention is that the photonic crystal disclosed has a porous body. However, nowhere in Hiraoka does it teach or suggest the desirability of incorporating a porous chip insulating layer in a multi-chip cube structure to reduce the dielectric constant of the insulating layer. It appears that the Examiner cited Hiraoka against Applicant's invention simply because Hiraoka discloses the use of a porous material even though the porous material is being used in a completely different context. Applicant respectfully submits the mere fact that a reference can be modified to include the limitations of the present invention does not make the modification obvious unless the prior art suggested the desirability of the modification. See *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992).

The same argument is applicable to the Examiner's rejection of Applicant's invention over Bertin in view of Hiraoka. In the July 16, 2003 Office Action, the Examiner indicated that Applicant's invention is obvious in light of Bertin in view of Hiraoka. While Bertin discloses a cube package of stacked silicon semiconductor chips, the Examiner has produced no prior art suggesting that the cube package disclosed in Bertin can be modified to include an insulating layer comprising a plurality of enclosed regions of air adapted to reduce the dielectric constant of the layer. As discussed above, the Hiraoka reference is directed toward a porous photonic crystal and thus does not appear to have much relevance other than that the material of the photonic crystal happens to be porous. Furthermore, nowhere in Bertin or Hiraoka does it suggest the desirability to incorporate a porous insulating layer in a multi-chip module for the purposes of reducing capacitive coupling between adjacent chips.

The Examiner also indicated that Applicant's invention is obvious in light of Bertin in view of Farrar. Bertin discloses a semiconductor chip stack in which adjacent chips are separated by insulating layers while Farrar discloses a method of forming foamed polymeric material. However, Bertin teaches away from forming voids in the insulating layer between chips in a chip stack as claimed by Applicant. In fact, Bertin suggests that voids in the insulating layer between chips in a chip stack can detrimentally affect bonding between chips. Specifically, Bertin emphasizes that his invention offers significant advantages by providing a *void-free* film of fully cured polyimide between chips of a stack and that associated with these voids are serious mechanical and reliability problems." (See, *e.g.*, column 8, lines 1-22 of Bertin, emphasis added)

In fact, one of the inventive features of Bertin appears to be directed toward preventing void formation as Bertin states in the specification that "[a]pplicants found and disclose in this application advantageous materials and methods to prevent void formation." (column 8, lines 6-8 of Bertin) Accordingly, there could have been no motivation or incentive to combine Bertin with Farrar to form foamed polymeric insulating layers when Bertin specifically teaches away from forming such voids in the insulating material.

A Section 103 rejection is improper if the "prior art of record fails to provide any suggestion or incentive." *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985) The Examiner's suggestion that these references should be combined is a classic case of using the benefit of hindsight as the Examiner has pointed to nothing in the prior art that suggests the desirability of combining the references. Furthermore, Applicant notes that "it is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claim as a blueprint." *Id.* As the Federal Circuit has noted, "Obviousness cannot be established by combining the teachings of the prior art to produce the invention, absent some teaching or suggestion supporting the combination. Under Section 103, teachings of references can be combined only if there is some suggestion or incentive to do so." *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1588 (Fed. Cir. 1984).

In summary, none of the references cited by the Examiner, either alone or in combination, teach a multi-chip structure incorporating a chip insulating layer having enclosed regions of air adapted to lower the dielectric constant of the insulating layer. As a consequence, Applicant respectfully submits that Claim Group I (Claims 1, 3, 5-10, 12-18) and Claim Group 2 (Claims 2, 4, 11, 19-26) are not made obvious under 35 U.S.C. §103 by any of the references cited by the Examiner.

B. Conclusion

Nothing in the prior art, individually or in combination, discloses, teaches, or suggests the inventions recited by the claims of Applicant's disclosure. Furthermore, the art recited by the Examiner fails to supply any motivation or suggestion to combine the applied references in the manner suggested by the Examiner. Applicant respectfully submits that the claimed invention is

patentably distinct over the prior art. In view of the foregoing, Applicant requests that the rejection of Claims 1-26 be reversed.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 12/15/2003

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